MVME2100
Single Board Computer

Programmer's Reference Guide

V2100A/PG2

June 2001 Edition

Printed in the United States of America.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution

Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.

Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatznur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

> EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class B
>
> EN55024 “Information technology equipment—Immunity characteristics—Limits and methods of measurement”

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

In accordance with European Community directives, a “Declaration of Conformity” has been made and is available on request. Please contact your sales representative.

Notice

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Motorola, Inc.
Computer Group
2900 South Diablo Way
Tempe, Arizona 85282

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About This Manual

The *MVME2100 Single Board Computer Programmer's Reference Guide* provides the information you will need to program and customize your MVME2100 Single Board Computer. It provides specific programming information and data applicable to the board.

As of the printing date of this manual, the MVME2100 is available in the configurations shown below.

Model	MPC	Memory	Handles
MVME2101-1	MPC8240 @200MHz	32MB SDRAM 5 MB Flash Memory	VME Scanbe
MVME2101-3		32MB SDRAM 5 MB Flash Memory	IEEE 1101 (Injector/Ejector)
MVME2112-1	MPC8240 @250MHz	64MB SDRAM 9 MB Flash Memory	VME Scanbe
MVME2112-3		64MB SDRAM 9 MB Flash Memory	IEEE 1101 (Injector/Ejector)

Summary of Changes

The following changes were made for the PG2 revision of this manual.

Date	Doc. Rev	Changes
06/2001	V2100A/PG2	A note was added to page 1-16 to explain PPCBug's use of Bit 7 for Flash Bank selection. This section "About this Manual" was also added.

Overview of Contents

The following paragraphs briefly describe the contents of each chapter.

Chapter 1, *Product Data and Memory Maps*, provides an overview of the MVME2100 including a table of key features and a block diagram. The remainder of the chapter includes a description of the Memory Maps including Processor Memory Map information, PCI Memory Map information, PCI I/O Memory Map information, and System I/O Memory Map information.

Chapter 2, *Programming Details*, provides PCI Arbitration information, Interrupt Handling information, EEPROM device ID and configuration information, and information on Input/Output functions, as well as a brief description of the memory characteristics of the MVME2100.

Appendix A, *Related Documentation*, provides a listing of related Motorola documentation, Manufacturer's or Third Party documentation, and related industry specifications.

Comments and Suggestions

Motorola welcomes and appreciates your comments on its documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

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Reader Comments DW164
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You can also submit comments to the following e-mail address:
reader-comments@mcg.mot.com

In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Terminology

A character precedes a data or address parameter to specify the numeric format, as follows (if not specified, the format is hexadecimal):

0x	Specifies a hexadecimal number
%	Specifies a binary number
&	Specifies a decimal number

An asterisk (*) following a signal name for signals that are *level significant* denotes that the signal is *true* or valid when the signal is low.

An asterisk (*) following a signal name for signals that are *edge significant* denotes that the actions initiated by that signal occur on high to low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

Byte	8 bits, numbered 0 through 7, with bit 0 being the least significant.
Half word	16 bits, numbered 0 through 15, with bit 0 being the least significant.
Word	32 bits, numbered 0 through 31, with bit 0 being the least significant.
Double word	64 bits, numbered 0 through 63, with bit 0 being the least significant.

Product Data and Memory Maps

1

Introduction

The MVME2100 is a “state-of-the-art” Single Board Computer. It is based on the MPC8240 Integrated Processor and includes support circuitry such as SDRAM, PROM/Flash memory, and bridge to the VMEbus.

Note Unless otherwise specified, the designation “MVME2100” refers to all models of the MVME2100-series Single Board Computers.

What this Guide Provides

This guide provides programming information and data applicable to the MVME2100. It also provides details of several programming functions applicable to the board.

It is important to note that unlike similar products, the MVME2100 incorporates an “Integrated Processor”. This means that many components typically found on the Printed Circuit Board (PCB) of other products, have been integrated into the MVME2100’s processor. A good example of this would be the board’s chip set.

Because the MVME2100 incorporates an integrated processor, much of the programming information and data normally found in the product’s programming reference manual(s) is located in the following documentation:

- MPC8240 Integrated Processor User’s Manual
- MPC603e and EC603e RISC Microprocessor User’s manual
- MPC8240 White Paper
- MPC8240 Technical Summary
- MPC8240 Processor Hardware Specifications
- MPC8240 Training Manual

The following table lists the key features of the MVME2100.

Table 1-1. MVME2100 Key Features

Processors	• MPC8240™ • Bus Clock Frequencies of 66.67 or 83.33 MHz
Flash Memory	• 1 MB via two 32-pin PLCC/CLCC Sockets for 1MB (8-bit); 4MB or 8MB surface mount (64-bit)
System Memory	• 32 or 64MB Synchronous DRAM
LAN	• DEC21143 10/100Base-TX Ethernet Controller • LXT970 Fast Ethernet Transceiver
Interrupt Controller	• PowerPC® Embedded Programmable Interrupt Controller (EPIC)
DMA	• 2 Independent DMA Channels
Timers	• Four, 16-bit programmable timers
I^2C®	• Integrated I^2C port with full master support
I_2O	• I_2O compliant messaging interface
NVRAM	• 8KB (MK48T59Y)
RTC & Watchdog Timer	• MK48T59 device • On Watchdog Timer, Time-out generates reset
Serial Interface	• One 16550-compatible asynchronous serial port
PCI Mezzanine Card	• One 32-bit PMC slot • Front panel I/O • MVME2300 compatible P2 I/O
PC-MIP™	• Two 32-bit Type I PC-MIP slots (MVME2300 compatible P2 I/O) • Two 32-bit Type II PC-MIP slots (front panel I/O)
PCI Expansion	• 114-pin connector located on the planar of the board (33 MHz)
Miscellaneous	• RESET switch • ABORT switch • Three LEDs for Fail, Activity, SCON
Form Factor	• Standard 6U VME

The following block diagram illustrates the architecture of the MVME2100 Single Board Computer.

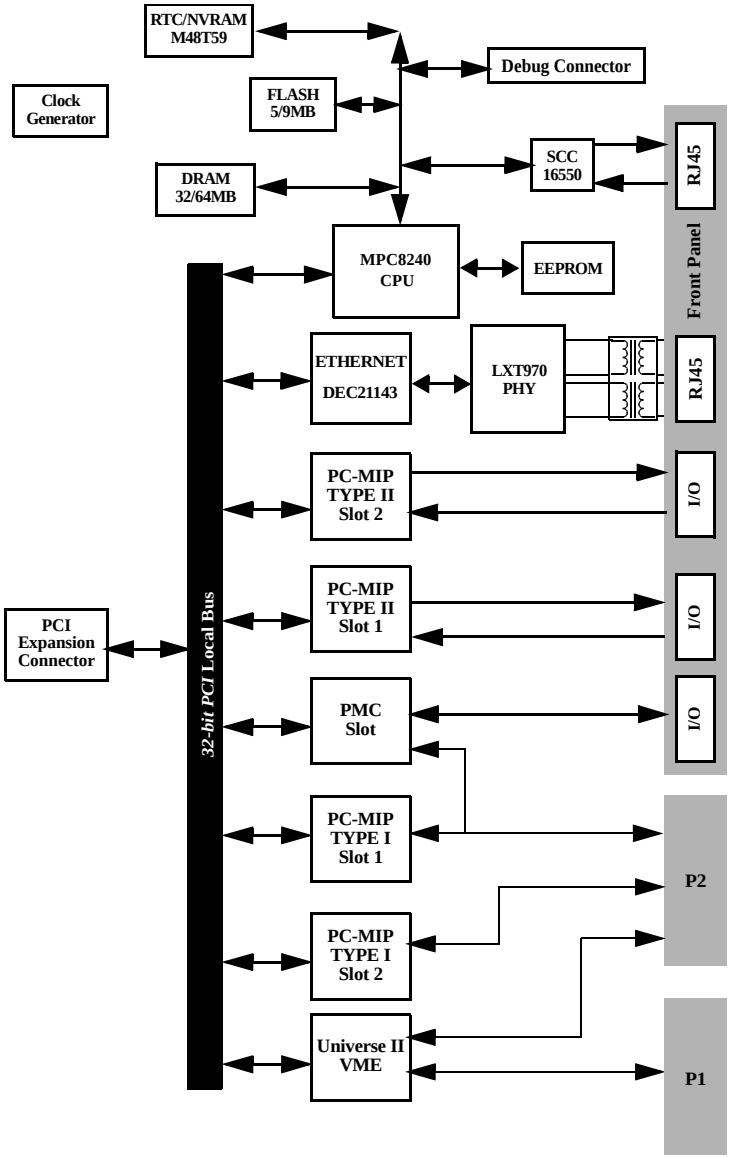

Figure 1-1. MVME2100 Block Diagram

Memory maps

The following sections describe the memory maps for the MVME2100.

Processor Memory Map

The Processor Memory Map is controlled by the Processor Peripheral device. The MPC8240 supports two address maps designated address Map A (PReP) and address Map B (CHRP). The MVME2100 defaults to address Map A when power is first applied or after a hard reset has occurred.

Address Map A (PReP)

When power is first applied or a hard reset has occurred the CPU board defaults to address Map A or the PReP memory map as shown in the following table.

Table 1-2. Processor Address Map A (PReP)

Processor Address		Size	Definition	Notes
Start	End			
0000 0000	7FFF FFFF	2G	System Memory Space	
8000 0000	807F FFFF	8M	PCI/ISA I/O Space	1,2
8080 0000	80FF FFFF	8M	PCI configuration direct accesses	3
8100 0000	BF7F FFFF	1G - 24M	PCI I/O Space	
BF80 0000	BFFF FFEF	16M	Reserved	
BFFF FFF0	BFFF FFFF	16M	PCI/ISA interrupt acknowledge	4
C000 0000	FEFF FFFF	1G - 16M	PCI Memory Space	
FF00 0000	FF7F FFFF	8M	ROM/FLASH Bank 1	5
FF80 0000	FF8F FFFF	1M	System I/O (Port X replicated)	
FF90 0000	FF9F FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFCA 0000	FFAF FFFF	1M	System I/O (Port X replicated)	

Table 1-2. Processor Address Map A (PReP) (Continued)

Processor Address		Size	Definition	Notes
Start	End			
FFB0 0000	FFBF FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFA0 0000	FFAF FFFF	1M	System I/O (Port X replicated)	
FFD0 0000	FFDF FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFE0 0000	FFEF FFFF	1M	System I/O (Port X)	
FFF0 0000	FFFF FFFF	1M	ROM/FLASH Bank 0	6

Notes

1. PCI configuration accesses to CF8 and CFC-CFF are handled as specified in the PCI Local Bus Specification. For additional information, refer to *PCI Configuration Space* in Chapter 2.

2. Processor addresses are translated to PCI addresses as follows:

In contiguous mode:

PCI address (AD31-0) = 0b0 || A[1-31]. PCI configuration accesses use processor addresses 80000CF8 and 80000CFC - 80000CFF.

In discontinuous mode:

PCI address (AD[31-0]) = 0x0000 || A[9-19] || A[27-31]. PCI configuration accesses use processor addresses 80067018 and 8006701C - 8006701F.

3. IDSEL for direct access method: 11 - 0x808008xx, 12 = 0x808010xx,..., 18 = 0x808400xx.

4. Reads to this address generate PCI interrupt-acknowledge cycles.

5. ROM/FLASH bank 1 may contain up to 8MB of 64-bit wide FLASH memory.

6. ROM/FLASH bank 0 may contain up to 1MB of FLASH memory on the MVME2100 and is accessed byte wide.

Address Map B (CHRP)

The system software may initialize the processor to use Address Map B. The following table shows the recommended CHRP Memory Map from the point of view of the Processor.

Table 1-3. Processor Address Map B (CHRP)

Processor Address		Size	Definition	Notes
Start	End			
0000 0000	top_dram	dram_size	System Memory (onboard DRAM)	1, 2
top_dram	7FFF FFFF	2G - dram_size	Reserved	
8000 0000	FCFF FFFF	2G - 48M	PCI Memory Space	3
FD00 0000	FDFF FFFF	16M	PCI/ISA Memory Space	
FE00 0000	FE7F FFFF	8M	PCI/ISA I/O Space	
FE80 0000	FEBF FFFF	4M	PCI I/O Space	
FEC0 0000	FEDF FFFF	2M	PCI Configuration address register	
FEE0 0000	FEEF FFFF	1M	PCI Configuration data register	
FEF0 0000	FEFF FFFF	1M	PCI Interrupt Acknowledge	4
FF00 0000	FF7F FFFF	8M	ROM/FLASH Bank 1	5
FF80 0000	FF8F FFFF	1M	System I/O (Port X replicated)	
FF90 0000	FF9F FFFF	1M	ROM/FLASH Bank 0 (replicated	
FFA0 0000	FFAF FFFF	1M	System I/O (Port X replicated)	
FFB0 0000	FFBF FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFC0 0000	FFCF FFFF	1M	System I/O (Port X replicated)	
FFD0 0000	FFDF FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFE0 0000	FFEF FFFF	1M	System I/O (Port X)	
FFF0 0000	FFFF FFFF	1M	ROM/FLASH Bank 0	6

Notes

1. Programmable via the processor's memory controller.
2. The processor should be initialized to ignore the compatibility hole address range of 0x000A 0000 - 0x000B FFFF by clearing the 'PROC_COMPATIBILITY_HOLE' bit in the Emulation Support configuration register.
3. CHRP requires the starting address for the PCI Memory Space to be 256M-aligned.
4. Reads to this address generate PCI interrupt-acknowledge cycles; writes to this address generate TEA* (if enabled).
5. ROM/FLASH bank 1 may contain up to 8MB of 64-bit wide FLASH memory.
6. ROM/FLASH bank 0 may contain up to 1MB of FLASH memory on the MVME2100 and is accessed byte wide.

PCI Memory Map

The PCI Memory Map is controlled by the processor peripheral device. The MPC8240 supports two address mapping configurations designated address Map A (PReP), address Map B (CHRP). The MVME2100 defaults to address map A when power is first applied or after a hard reset has occurred.

PCI Memory Map A (PReP)

The following table shows address Map A from the PCI memory master view.

Table 1-4. PCI Memory Master View (PReP)

PCI Address		Size	Definition	Notes
Start	End			
0000 0000	00FF FFFF	16M	PCI/ISA Memory	
0100 0000	7EFF FFFF	2G - 16M	PCI Memory	
7F00 0000	7FFF FFFF	16M	Reserved	
8000 0000	FFFF FFFF	2G	System Memory Space	

PCI Memory Map B (CHRP)

The following table shows address Map B from the PCI memory master view.

Table 1-5. PCI Memory Master View (CHRP)

PCI Address		Size	Definition	Notes
Start	End			
0000 0000	top_dram	dram_size	System Memory (onboard DRAM)	1
top_dram	3FFF FFFF	1G - dram_size	Not Used	
4000 0000	7FFF FFFF	1G	Reserved	
8000 0000	FCFF FFFF	2G - 48M	PCI Memory Space	
FD00 0000	FDFF FFFF	16M	System Memory Space	
FE00 0000	FEFF FFFF	16M	Reserved	
FF00 0000	FF7F FFFF	8M	ROM/FLASH Bank 1	2
FF80 0000	FF8F FFFF	1M	System I/O (Port X)	
FF90 0000	FF9F FFFF	1M	ROM/FLASH Bank 0	3
FFA0 0000	FFAF FFFF	1M	System I/O (Port X replicated)	
FFB0 0000	FFBF FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFC0 0000	FFCF FFFF	1M	System I/O (Port X replicated)	
FFD0 0000	FFDF FFFF	1M	ROM/FLASH Bank 0 (replicated)	
FFE0 0000	FFEF FFFF	1M	System I/O (Port X replicated)	
FFF0 0000	FFFF FFFF	1M	ROM/FLASH Bank 0 (replicated)	

Notes

1. The processor should be initialized to ignore the compatibility hole address range of 0x000A 0000 - 0x000F FFFF by clearing the ‘PCI_COMPATIBILITY_HOLE’ bit in the Emulation Support configuration register.

2. ROM/FLASH bank 1 may contain up to 8MB of 64-bit wide FLASH memory.

3. ROM/FLASH bank 0 may contain up to 1MB of FLASH memory on the MVME2100 and is accessed byte wide.

PCI I/O Memory Map

The PCI I/O Memory Map is controlled by the processor peripheral device. The MPC8240 supports two address mapping configurations designated address Map A (PReP), address Map B (CHRP). The MVME2100 defaults to address map A when power is first applied or after a hard reset has occurred.

PCI I/O Map A (PReP)

The following table shows address Map A from the PCI I/O master view.

Table 1-6. PCI I/O Address Map A (PReP)

PCI Address		Size	Definition
Start	End		
0000 0000	0000 FFFF	64K	ISA/PCI I/O Space
0001 0000	007F FFFF	8M - 64K	Reserved
0080 0000	3F7F FFFF	1G - 16M	PCI I/O Space
3F80 0000	3FFF FFFF	8M	Reserved
4000 0000	FFFF FFFF	3G	Reserved

PCI I/O Map B (CHRP)

The following table shows address Map B from the PCI I/O master view. The MPC8240 does not respond to PCI I/O cycles when in the PCI host bridge mode.

Table 1-7. PCI I/O Address Map B (CHRP)

PCI Address		Size	Definition
Start	End		
0000 0000	0000 FFFF	64K	PCI/ISA I/O Space
0001 0000	007F FFFF	8M - 64K	Reserved
0080 0000	3F7F FFFF	1G - 8M	PCI I/O Space
3F80 0000	FFFF FFFF	3G + 8M	Reserved

System I/O Memory Map

System resources for the MVME2100 including system control and status registers, NVRAM/RTC, and the 16550 UART are mapped into the lower 1MB address range of FLASH/ROM bank 0 (0xFFE00000 - 0xFFEFFFFF). The following table shows the system I/O memory map for the MVME2100.

Table 1-8. System I/O Memory Map

Address		Size	Definition	Notes
Start	End			
FFE0 0000	FFE0 0FFF	4K	System Status Register 1	1
FFE0 1000	FFE0 1FFF	4K	System Status Register 2	1
FFE0 2000	FFE0 2FFF	4K	PCI Presence Detect Register	1
FFE0 3000	FFE0 3FFF	4K	Geographical Address Register	2
FFE0 4000	FFE0 4FFF	4K	Configuration Header Register	2
FFE0 5000	FFE0 7FFF	12K	Reserved for onboard registers	
FFE0 8000	FFE0 8FFF	4K	SIMM/DIMM 0 Parallel Presence Detection Register	3
FFE0 9000	FFE0 9FFF	4K	SIMM/DIMM 1 Parallel Presence Detection Register	3
FFE0 A000	FFE0 AFFF	4K	SIMM/DIMM 2 Parallel Presence Detection Register	3
FFE0 B000	FFE0 BFFF	4K	SIMM/DIMM 3 Parallel Presence Detection Register	3
FFE0 C000	FFE0 FFFF	16K	Reserved	
FFE1 0000	FFE1 0FFF	4K	COM1 16550 UART	1
FFE1 1000	FFE1 1FFF	4K	COM2 16550 UART	3
FFE1 2000	FFE1 2FFF	4K	COM3 16550 UART	3
FFE1 3000	FFE1 3FFF	4K	COM4 16550 UART	3
FFE1 4000	FFE1 7FFF	16K	Reserved	

Table 1-8. System I/O Memory Map (Continued)

Address		Size	Definition	Notes
Start	End			
FFE1 8000	FFE1 8FFF	4K	IEEE1284 Parallel Interface Port	3
FFE1 9000	FFE1 FFFF	28K	Reserved	
FFE2 0000	FFE2 0FFF	4K	SCC (85230)	3
FFE2 1000	FFE7 EFFF	376K	Reserved (undefined)	
FFE7 F000	FFE7 FFFF	4K	NVRAM Page Register	3,4
FFE8 0000	FFEF FFFF	512K	NVRAM/RTC	1,5

Notes

1. Recommended function for all MPC8240 based designs.
2. Optional function implemented on the MVME2100.
3. Optional function not implemented on the MVME2100.
4. Only required if more than 512KB of NVRAM is implemented.
5. The MVME2100 implements 8KB of NVRAM.

System Status Register 1

The MVME2100 contains a System Status Register that may be used to generate a hard reset to the board, to control status indicators, and to provide a reference clock for the CPU. The following table provides the necessary information on the System Status Register 1.

Table 1-9. System Status Register 1

REG	System Status Register 1- 0xFFE00XXX							
BIT	0	1	2	3	4	5	6	7
FIELD	RESET	RSVD	RSVD	ABORT	EEPROM_WP	FLASH_WP	FLASH_BSY	REF_CLK
OPER	R/W			R	R/W			R
RESET	0	0	0	X	0	0	X	X

RESET Setting this bit will force a hard reset of the MVME2100. This bit will always be cleared during a read.

ABORT This bit reflects the current state of the onboard abort signal. This is a debounced version of the abort switch and may be used to determine the state of the abort switch. A set condition indicates that the abort switch is not depressed while a cleared condition would indicate that the abort switch had been recently activated.

EEPROM_WP EEPROM Write Protect. This bit is to provide protection against inadvertent writes to the onboard EEPROM devices. This bit is cleared during reset and must be set by the system software to provide write protection for the EEPROMs.

FLASH_WP FLASH Write Protect. This bit is to provide protection against inadvertent writes to the FLASH memory devices. This bit is cleared during reset and must be set by the system software to provide write protection to the FLASH devices.

FLASH_BSY FLASH Busy. This bit reflects the current state of the RDY/BSY* signal of the expansion FLASH devices.

REF_CLK Reference Clock. This bit reflects the current state of the BAUDOUT clock from the COM1 16550 UART and may be used as a timing reference.

System Status Register 2

The MVME2100 contains a System Status Register that may be used to generate a hard reset to the board, to control status indicators, and to provide a reference clock for the CPU. The following table provides the necessary information on the System Status Register 2.

Table 1-10. System Status Register 2

REG	System Status Register 2- 0xFFE01XXX							
BIT	0	1	2	3	4	5	6	7
FIELD	BD_FAIL	LED_1	LED_2	LED_3	LED_4	RSVD	RSVD	RSVD
OPER	R/W							
RESET	1	1	1	1	1	x	X	X

BD_FAIL Board Fail. This bit is used to control the Board Fail LED located on the front panel. A set condition illuminates the front panel LED and a cleared condition extinguishes the front panel LED.

LED_1 - LED_4 Reserved for future status indicators. A set condition illuminates the associated LED and a cleared condition extinguishes the LED.

PCI Presence Detect Register

The MVME2100 contains a PCI Presence Detect Register that may be read by the system software to determine the presence of optional PCI devices. The following table provides the necessary information on the PCI Presence Detect Register.

Table 1-11. PCI Presence Detect Register

REG	PCI Presence Detect Register - 0xFFE02XXX							
BIT	0	1	2	3	4	5	6	7
FIELD	PRSNT8	PRSNT7	PRSNT6	PRSNT5	PRSNT4	PRSNT3	PRSNT2	PRSNT1
OPER	R							
RESET	X	1	1	1	X	X	X	X

PRSNT8 A cleared condition indicates the presence of a PMC Carrier board connected to the PCI expansion connector. While a set condition indicates the absence of the PMC Carrier board.

PRSNT7-5 Reserved for future PCI devices.

PRSNT4 A cleared condition indicates the presence of a board in the PC-MIP Type II slot 2. While a set condition indicates the absence of a board in the PC-MIP Type II slot 2.

PRSNT3 A cleared condition indicates the presence of a board in the PC-MIP Type II slot 1. While a set condition indicates the absence of a board in the PC-MIP Type II slot 1.

PRSNT2 A cleared condition indicates the presence of a board in the PC-MIP Type I slot 2. While a set condition indicates the absence of a board in the optional PC-MIP Type I slot.

PRSNT1 A cleared condition indicates the presence of a board in the optional PMC/PC-MIP slot. While a set condition indicates the absence of a board in the optional PMC/PC-MIP slot.

VMEbus Geographical Address Register

The MVME2100 contains a VMEbus Geographical Address register that may be read by the system software to determine the VMEbus board slot that the MVME2100 is plugged into. The following table provides the necessary information on the VMEbus Geographical Address Register.

Table 1-12. VMEbus Geographical Address Register

REG	VMEbus Geographical Address Register - 0xFFE03XXX							
BIT	0	1	2	3	4	5	6	7
FIELD	RSVD	RSVD	VMEGAP*	VMEGA4*	VMEGA3*	VMEGA2*	VMEGA1*	VMEGA0*
OPER	R							
RESET	X	X	X	X	X	X	X	X

VMEGAP* VMEbus Geographical Address Parity. This bit is used to generate an odd geographical address parity.

VMEGA[0-4]* VMEbus Geographical Address bits may be used by the system software to determine which slot in a VME/64 VMEbus backplane that the board has been installed in. The value read will be the inverse of the slot number into which the board is plugged. A value of 0x1F indicates that VME Geographical addressing is not supported.

Configuration Header Register

The MVME2100 contains an 8-bit user defined header that may be read by the software. The following table provides the necessary information on the Configuration Header Register.

Table 1-13. Configuration Header Register

REG	Configuration Header Register - 0xFFE04XXX							
BIT	0	1	2	3	4	5	6	7
FIELD	CFG_0	CFG_1	CFG_2	CFG_3	CFG_4	CFG_5	CFG_6	CFG_7
OPER	R							
RESET	X	X	X	X	X	X	X	X

CFG[0-7] Configuration Bits 0-7. These bits reflect the presence of the jumpers installed on the configuration header. A cleared condition indicates the presence of a jumper in the header position associated with that bit and a set condition indicates the absence of a jumper in the header position associated with the bit.

Note Bit 7 is reserved by PPCBug to select which flash bank to boot from.
ON = Continue the boot process from Bank A
OFF = Start from, and continue from, Bank B
The MPC8240 embedded processor requires that this hardware always start the boot process from Flash Bank B. If Bit 7 is ON, PPCBug will attempt to pass the board initialization and boot control over to Flash Bank A. If Bit 7 is OFF, the boot process will start and finish from Flash Bank B.

SIMM/DIMM Parallel Presence Detection Registers

These registers are reserved for future implementations of MPC8240 based systems and are intended for boards containing SIMM or DIMM memory sockets using a parallel presence detection scheme.

Note These registers are not implemented on the MVME2100. Attempts to read these registers will result in indeterminate data being returned.

Table 1-14. SIMM/DIMM Parallel Presence Detection Registers

REG	SIMM/DIMM Parallel Presence Detection Registers - 0xFFE08XXX-0xFFE0BXXX							
BIT	0	1	2	3	4	5	6	7
FIELD	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
OPER	R							
RESET	x	x	X	X	X	X	X	X

PD[0-7] These bits reflect the current state of the presence detect bits of any installed SIMM/DIMM modules that used a parallel presence detection scheme.

Programming Details

2

Introduction

This chapter provides details of several programming functions applicable to the MVME 2100 Single Board Computer.

PCI Arbitration

PCI arbitration for the MVME 2100 is provided by the integrated PCI arbiter internal to the MPC8240 processor in conjunction with an external sub-arbiter.

The processor provides support for itself and up to 5 external PCI masters. Since the MVME 2100 could have as many as seven potential PCI masters in addition to the MPC8240, an onboard sub-arbiter is provided. The sub-arbiter is designed to multiplex the common PMC/PC-MIP slot and three dedicated PC-MIP slots onto two of the MPC8240 PCI bus request/grant pins as shown in the figure below:

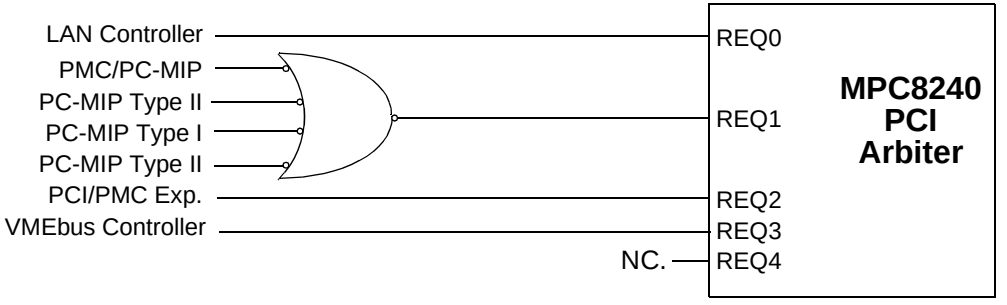

Figure 2-1. MVME 2100 PCI Arbitration

2

Interrupt Handling

The MVME 2100 uses the Embedded Programmable Interrupt Controller (EPIC) integrated into the processor to manage locally generated interrupts. The interrupt controller will operate in the serial interrupt mode. Currently defined external interrupting devices and serial interrupt assignments are shown in the table below:

Table 2-1. Serial Interrupt Assignments

Serial Interrupt No.	Edge/ Level	Polarity	Interrupt Source	Notes
0	N/A	N/A	Not Used	1
1	Level	Low	DEC21143 Controller	
2	Level	Low	PMC/PC-MIP Type I Slot 0	
3	Level	Low	PC-MIP Type I Slot 1	
4	Level	Low	PC-MIP Type II Slot 0	
5	Level	Low	PC-MIP Type II Slot 1	
6	N/A	N/A	Not Used	1
7	Level	Low	PCI Expansion Interrupt A/Universe II (LINT0)	2
8	Level	Low	PCI Expansion Interrupt B/Universe II (LINT1)	2
9	Level	Low	PCI Expansion Interrupt C/Universe II (LINT2)	2
10	Level	Low	PCI Expansion Interrupt D/Universe II (LINT3)	2
11	N/A	N/A	Not Used	1
12	N/A	N/A	Not Used	1
13	Level	High	16550 UART	
14	Edge	Low	Front panel Abort Switch	
15	Level	Low	RTC IRQ	

Notes 1. Interrupts 0, 6, 11, and 12 are not used and should be disabled by setting the priority to zero in processor's Serial Interrupt Source/Vector Priority Registers.

2. Interrupts 7-10 are shared between the PCI INTA-D and the Universe II VMEbus local interrupts 0-3 as shown. Universe II local interrupts 4-7 are not used.

EEPROM Functionality

The following table shows the EEPROMs used for the MVM2100 and their assigned device IDs.

Table 2-2. System EEPROM Device IDs

EEPROM ID	Size (bytes)	Function
000	256	SDRAM Bank 0
001	256	SDRAM Bank 1
010	256 (max)	Reserved for additional memory banks
011	256 (max)	Reserved for additional memory banks
100	256	System Configuration Data
101	256 (max)	Undefined
110	256 (max)	Undefined
111	256 (max)	Undefined

SDRAM Configuration EEPROM

EEPROMs are used on the MVME2100 to contain information regarding the SDRAM devices installed. The data is formatted in accordance to JEDEC standard JESD21-C. The information contained in these EEPROM(s) will be used by the system software to configure the memory controller function integrated into the MPC8240 peripheral device.

System Configuration EEPROM

The MVME2100 also contains an EEPROM containing configuration information specific to the board. Typical information that may be present in this device is: manufacturer, board revision, build version, date of assembly, memory present, options present, L2 cache information, etc.

The EEPROM is hardwired to have a device ID of 0b100 and this ID will not be used for any other function.

2

Input/Output Functionality

Ethernet Controller

The MVME2100 provides one optional 10/100Base-TX Ethernet interface port implemented using a DEC21143 Ethernet Controller and a LXT970 Fast Ethernet Transceiver. The 10/100Base-TX is interfaced via an industry standard RJ45 connector located on the front panel of the MVME2100.

The presence of the DEC21143 device can be positively determined by reading the contents of the System Configuration EEPROM described earlier.

PMC/PC-MIP Type I Expansion Slot

As a factory option the MVME2100 may be populated to support either one PCI Mezzanine Card slot or one PC-MIP Type I PCI slot for user-defined functions.

The PCI interrupts signals INTA#, INTB#, INTC#, and INTD# for this slot are hardwired together and connected to the onboard Interrupt Controller.

PC-MIP Type I Expansion Slot

In addition to the PMC/PC-MIP Type I slot, the MVME2100 will have one dedicated PC-MIP Type I card slot for user defined functions.

The PCI interrupts signals INTA#, INTB#, INTC#, and INTD# for this slot are hardwired together and connected to the onboard Interrupt Controller.

PC-MIP Type II Expansion Slots

The MVME2100 has two dedicated PC-MIP Type II card slots for user defined functions.

The PCI interrupts signals INTA#, INTB#, INTC#, and INTD# for each of these slots are hardwired together and connected to the onboard Interrupt Controller.

VMEbus Interface

The VMEbus interface for the MVME2100 board is provided by the Universe ASIC. Refer to the *Universe User's Manual* for additional information.

PCI/PMC Expansion Capability

The MVME2100 provides additional PCI/PMC capability through the use of a 114-pin Mictor connector that is compatible with other VMEbus processor boards. By using existing PMCspan carrier boards up to four additional PMC boards can be used.

The PCI interrupts signals INTA#, INTB#, INTC#, and INTD# for these PCI/PMC expansion board(s) are separately connected to the MPC8240 serial Interrupt Controller.

PCI Configuration Space

When using Address Map A, the PCI configuration registers are accessed by an indirect method in accordance to the PCI Local Bus Specification. The register address is written to CONFIG_ADDR at 0x8000 0CF8. Then the data is accessed at CONFIG_DAT at addresses 0x8000 0CFC - 0x8000 0CFF.

When using Address map B, the PCI configuration registers are accessed in a similar manner except CONFIG_ADDR is located at any word-aligned address in the range 0xFEC0 0000 through 0xFEDF FFFF and CONFIG_DAT is located at any word-aligned address in the range 0xFEE0 0000 through 0xFEEF FFFF.

Each PCI device has an associated address line connected via a resistor to its IDSEL pin for Configuration Space accesses. The table below shows the IDSEL assignments for the PCI devices on the MVME2100.

Table 2-3. IDSEL Mapping for PCI Devices

Device Number Field	PCI Address Line	Physical PCI Device
0b0_1101	AD13	Universe II PCI-VMEbus
0b0_1110	AD14	DEC21143 Controller
0b1_0000	AD16	PMC/PC-MIP Type I Slot 0
0b1_0001	AD17	PC-MIP Type I Slot 1
0b1_0010	AD18	PC-MIP Type II Slot 0
0b1_0011	AD19	PC-MIP Type II Slot 1

2

Memory Characteristics

System Memory

System memory for the MVME2100 is provided by 2 banks of synchronous DRAM. Each bank consists of five 4Mx16 SDRAM devices providing a 32MB bank organized in a 4Mx72 configuration.

This design allows memory configurations of 32 or 64MB that can be supported by the MVME2100.

During system initialization the firmware will determine the presence of, and configuration of each memory bank installed by reading the contents of the serial presence detect ROM (located on the MVME2100). The system firmware initializes the MPC8240 Memory Controller for proper operation based on the contents of the serial presence detection ROM.

FLASH Memory

The MVME2100 contains two banks of FLASH memory accessed via the integrated memory controller contained within MPC8240. Bank 0 consists of two 32-pin PLCC sockets that can be populated with up to 1024KB of FLASH memory, resides at address 0xFFF00000- 0xFFFFFFFF and is restricted to 8 bits in width.

Bank 1 may contain up to 8MB of 64-bit wide Boot Block FLASH memory devices. The following table shows typical memory sizes and device IDs:

Table 2-4. FLASH Memory Configurations

Bank Size (bytes)	Device ID
4MB	0x225B
4MB	0x22DA
8MB	0x2249
8MB	0x22C4

Related Documentation A

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature

Table A-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
MVME2100 Single Board Computer Installation and Use Manual	MVME2100A/IH
PPCBug Firmware User's Manual, Part 1 of 2	PPCBUGA1/UM
PPCBug Firmware User's Manual, Part 2of 2	PPCBUGA2/UM
PPCBug Diagnostics Manual	PPCDIAA/UM
MPC8240 Integrated Processor Training Manual (see note below)	N/A*
PMCspan PMC Adapter Carrier Module Installation and Use	PMCSPANA/IH

To obtain the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

Note The MPC8240 Integrated Processor Training Manual is the manual provided in MPC8240 Integrated Processor training class. Contact Motorola Computer Group Training Department for Manual and course availability.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. For your convenience, a source for the listed document is also provided.

Note In many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-2. Manufacturers' Documents

Document Title	Publication Number
MPC8240 Integrated Processor User's Manual Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140	MPC8240UM/D
MPC8240 White Paper Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140	MPC8240WP
MPC8240 Technical Summary Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140	MPC8240/D
MPC8240 Processor Hardware Specifications Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140	MPC8240EC
PowerPC 603 RISC Microprocessor User's Manual Motorola Literature Distribution Center Telephone: (800) 441-2447 or (303) 675-2140	MPC603EUM/AD
Universe II User Manual Tundra Semiconductor Corporation 603 March Road, Kanata, ON, Canada K2K 2M5 1-800-267-7231, (613) 592-0714, Fax: (613) 592-1320	N/A
TL16C550C Universal Asynchronous Receiver/Transmitter Texas Instruments Dallas, Texas	SLLS177C

Table A-2. Manufacturers' Documents (Continued)

Document Title	Publication Number
AM29LV800B 8Megabit CMOS 3.0 Volt-only Boot Sector Flash Memory Advanced Micro Devices Inc. P.O. Box 3453 Sunnyvale, California 94088-3453, (408) 732-2400	21490
AM29LV160B 16Megabit CMOS 3.0 Volt-only Boot Sector Flash Memory Advanced Micro Devices Inc. P.O. Box 3453 Sunnyvale, California 94088-3453, (408) 732-2400	21358
LXT970 Fast Ethernet Transceiver Level One Communications, Inc. 9760 Goethe Road Sacramento, CA 95827	N/A
AT24C01A/02/04/08/16 2-Wire Serial CMOS E^2PROM Atmel Corporation 2325 Orchard Parkway San Jose, CA 95131, (408) 441-0311	0180C
M48T59Y CMOS 8Kx8 Timekeeper SRAM SGS Thomson Microelectronics 1000 East Bell Road Phoenix, AZ 85022	M48T59Y
DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller, Hardware Reference Manual Digital Equipment Corp. Maynard, Massachusetts	EC-QWC4E-TE
DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Data Sheet Digital Equipment Corp. Maynard, Massachusetts	EC-QWC3C-TE

Related Specifications

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided.

Note In many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3. Related Specifications

Document Title and Source	Publication Number
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc. Publication and Sales Department 345 East 47th Street New York, New York 10017-21633 Telephone: 1-800-678-4333	P1386.1 Draft 2.0
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0 PCI Special Interest Group P.O. Box 14070 Portland, Oregon 97214-4070 Marketing/Help Line Telephone: (503) 696-6111 Document/Specification Ordering Telephone: 1-800-433-5177or (503) 797-4207 FAX: (503) 234-6762	PCI Local Bus Specification
Intelligent I/O (I_2O) Architecture Specification Version 1.5 March 1997 I_2O Special Interest Group 404 Balboa Street San Francisco, CA 94118 Voice: 415-750-8352 Fax: 415-751-4829	N/A

Table A-3. Related Specifications (Continued)

Document Title and Source	Publication Number
PC-MIP Specification VITA Standards Organization 7825 East Gelding Drive, Suite 104, Scottsdale AZ 85260	VITA 29 Draft 0.9a
PCI Mezzanine Card Specification IEEE Standards Department 445 Hoes Lane P.O Box 1331 Piscataway, NJ 08855-1331	P1386.1 Draft 2.0
Common Mezzanine Card Specification IEEE Standards Department 445 Hoes Lane P.O Box 1331 Piscataway, NJ 08855-1331	P1386 Draft 2.0
PCI Interface Specification Rev 2.1 PCI Special Interest Group 503-696-2000	PCI Rev 2.1

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For information on what services are available, or to purchase a support contract, call us at Services Central, at 1-800-624-6745 or 602-438-5875, or visit our web site at visit http://www.motorola.com/computer/support.

Glossary

Acronyms and Abbreviations

The following table explains some of the abbreviations, acronyms, and key terms used in this document.

Term	Meaning
ASIC	Application Specific Integrated Circuit
CHRP	(PowerPC) Common Hardware Reference Platform
CPU	Central Processing Unit
DIMM	Dual In-line Memory Module
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EPIC	Embedded Programmable Interrupt Controller
F/W	Firmware
H/W	Hardware
IEEE	Institute of Electrical and Electronics Engineers
I^2C	Inter IC
I_2O	Intelligent Input Output
I/O	Input/Output
ISA	Industry Standard Architecture
KB	Kilobytes
MB	Megabytes

Term	Meaning
MHz	Megahertz
NVRAM	Non-Volatile Random Access Memory
PCI	Peripheral Component Interconnect
PLCC	Plastic Leaded Chip Carrier
PMC	PCI Mezzanine Card (IEEE P1386.1)
PReP	PowerPC Reference Platform
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real-Time Clock
SBC	Single Board Computer
SCC	Serial Communication Controller
SDRAM	Synchronous Dynamic Access Memory
SIMM	Single In-line Memory Module
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
S/W	Software
TBGA	Tape Ball Grid Array
UART	Universal Asynchronous Receiver/Transmitter
VPD	Vital Product Data

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